AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-64. (canceled)

65. (currently amended) A memory controller comprising:

a first channel control circuit configured to couple to a first channel to access a first memory section, the first channel control circuit including programmable first registers to indicate starting and ending addresses for chip select mapping of the first memory section;

a second channel control circuit configured to couple to a second channel to access a second memory section, the second channel control circuit including programmable second registers to indicate starting and ending addresses for chip select mapping of the second memory section, wherein the second channel is independent of and separate from the first channel; and

~~one or more registers programmable with a first indication of whether or not the first channel and the second channel are interleaved~~

a programmable channel register in each of the first and second channel control circuits to be programmed to indicate that the first and second channels are to be interleaved when mapped, the interleaved channels to be mapped into sub-regions of one or more chip select mapped regions.

66. (currently amended) The memory controller as recited in claim 65 wherein ~~the first indication identifies which portion of an address received by the memory controller is used to select between the first and second channel if the first and second channel are interleaved~~ an address bit is to be used to select between the interleaved first and second channels.

67. (currently amended) The memory controller as recited in claim 65 ~~further comprising a plurality of channel control circuits including the first channel control circuit and the second channel control circuit, wherein the first indication further indicates whether or not other ones of the plurality of channel control circuits are interleaved~~ wherein an address bit, that is less significant than address bits that are to determine the one or more chip select mapped regions, is to be used to select between the interleaved first and second channels.

68. (currently amended) The memory controller as recited in claim ~~65 wherein the first channel includes a plurality of chip select signals, wherein each of the plurality of chip select signals corresponds to a different subsection of the first memory section, and wherein the first channel control circuit is configured to activate one of the plurality of chip select signals in response to an address received by the memory controller if the address is mapped to the first memory section~~ 66 wherein one or more of the chip select mapped regions are also interleaved.

69-77 (canceled)

78. (currently amended) A system comprising:

a processor configured to transmit an address of a memory location to be accessed; and

a memory controller coupled to receive the address from the processor, wherein the memory controller ~~is configured to couple to a memory including the memory location using at least a first channel and a second channel that is separate from and independent of the first channel, and wherein the memory controller is programmable with a first indication of whether or not the first channel and the second channel are interleaved~~ further comprises:

i) a first channel control circuit configured to couple to a first channel to access a first memory section, the first channel control circuit including programmable first registers to indicate starting and ending addresses for chip select mapping of the first memory section;

ii) a second channel control circuit configured to couple to a second channel to access a second memory section, the second channel control circuit including programmable second registers to indicate starting and ending addresses for chip select mapping of the second memory section, wherein the second channel is independent of and separate from the first channel; and

iii) a programmable channel register in each of the first and second channel control circuits to be programmed to indicate that the first and second channels are to be interleaved when mapped, the interleaved channels to be mapped into sub-regions of one or more chip select mapped regions.

79. (currently amended) The system as recited in claim 78 wherein ~~the first indication identifies which portion of the address received by the memory controller is used to select between the first channel and the second channel if the channels are interleaved~~ an address bit is to be used to select between the interleaved first and second channels.

80. (currently amended) The system as recited in claim 78 wherein ~~the memory controller is further configured to couple to a plurality of separate and independent channels including the first channel and the second channel, wherein the first indication further indicates whether or not other ones of the plurality of channels are interleaved~~ an address bit, that is less significant than address bits that are to determine the one or more chip select mapped regions, is to be used to select between the interleaved first and second channels.

81. (currently amended) The system as recited in claim ~~78 wherein the first channel includes a plurality of chip select signals, wherein each of the plurality of chip select signals corresponds to a different subsection of a first memory section coupled to the first channel during use, and wherein the memory controller is configured to activate one of the plurality of chip select signals in response to the address if the address is mapped to the first memory section~~ 79 wherein one or more of the chip select mapped regions are also interleaved.

82-90. (canceled)